

CLAIMS

1. In a content addressable memory (CAM) array having CAM cells arranged in rows of word lines and columns of data lines, a CAM cell, comprising:

a bistable circuit coupled to a power supply and ground, the bistable circuit having first and second data nodes;

first and second access transistors coupled to the first and second data nodes and first and second data lines, all respectively, for coupling the respective data node to the respective data line in response to activating a word line;

first and second capacitors, each capacitor having a first terminal coupled to a respective data node and having a second terminal coupled to ground; and

a match circuit having a search node coupled to the first data line, a cell node coupled to the first data node, and a match node coupled to a match line, the match circuit changing the logic state of the match line in response to search data provided on the first data line and the data stored at the first data node are mismatching.

2. The CAM array of claim 1 wherein the match circuit comprises:

first and second transistors coupled in series between the first and second data lines, the first transistor having a gate coupled to the first data node and the second transistor having a gate coupled to the second data node; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

3. The CAM cell of claim 1 wherein the bistable circuit comprises:

a first switch having a first node coupled to the first data node, a second node coupled to ground, and a control node coupled to the second data node;

a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

4. The CAM cell of claim 1 wherein the first and second data nodes store complementary data, and the first and second data lines are a pair of complementary data lines.

5. The CAM cell of claim 1 wherein the search data and the data stored at the first data node are mismatching when the logic level of each are the same.

6. In a content addressable memory (CAM) array having CAM cells arranged in rows of word lines and columns of data lines, a CAM cell, comprising:

a first bistable circuit coupled to a power supply and ground, the first bistable circuit having first and second data nodes;

a second bistable circuit coupled to the power supply and ground, the second bistable circuit having third and fourth data nodes;

first and second access transistors coupled to the first and second data nodes and first and second data lines, all respectively, for coupling the respective data node to the respective data line in response to activating a word line;

second and fourth access transistors coupled to the third and fourth data nodes and third and fourth data lines, all respectively, for coupling the respective data node to the respective data line in response to activating the word line;

first, second, third, and fourth capacitors, each capacitor having a first terminal coupled to a respective data node and having a second terminal coupled to ground; and

a match circuit having a first search node coupled to the first data line and a second search node coupled to the third data line, a first cell node coupled to the first data node and a second cell node coupled to the third data node, and a match node coupled to a match line, the match circuit changing the logic state of the match line in response to search data provided on

the first data line and the first data node mismatch and search data provided on the third data line and the third data node mismatch.

7. The CAM cell of claim 6 wherein the match circuit comprises first, second, third, and fourth switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node, and the third switch having its first node coupled to ground and its second node coupled to the match line, and the fourth switch having its first node coupled to the third data line, its second terminal coupled to the control terminal of the third switch, and its control node coupled to the third data node.

8. The CAM cell of claim 6 wherein the match circuit comprises first, second, third, and fourth switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor, and the third switch having its control terminal coupled to the third data node and its first node coupled to ground, the fourth switch having its control terminal coupled to the third data line, its first node coupled to the match line, and its second node coupled to the second node of the third transistor.

9. The CAM cell of claim 6 wherein the first and second bistable circuits comprise:

a first switch having a first node coupled to a true data node, a second node coupled to ground, and a control node coupled to a not data node;

a second switch having a first node coupled to the not data node, a second node coupled to ground, and a control node coupled to the true data node;

a first resistor having a first terminal coupled to the power supply and a second terminal coupled to the true data node; and

a second resistor having a first terminal coupled to the power supply and a second terminal coupled to the not data node.

10. The CAM cell of claim 6 wherein the first and second data nodes store complementary data, the first and second data lines are a pair of complementary data lines, the third and fourth data nodes store complementary data, and the third and fourth data lines are a pair of complementary data lines.

11. The CAM cell of claim 6 wherein the search data and the data stored at the first data node are mismatching when the logic level of each are the same.

12. A static content addressable memory array for a content addressable memory (CAM) device, comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit discharging a match line in response to a data value stored at the data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

13. The static CAM array of claim 12 wherein the match circuit comprises:
first and second transistors coupled in series between the data lines to which the
first and second access transistors are coupled, the first transistor having a gate coupled to a first
one of the data nodes and the second transistor having a gate coupled to a second one of the
complementary data nodes; and
a discharge transistor coupled between the match line and ground, and having a
gate coupled to a node between the first and second transistors.

14. The static CAM array of claim 12 wherein the latch is a first latch, the
match circuit is a first match circuit, and the static CAM array further comprises:
a second latch having complementary data nodes capacitively coupled to ground,
the first and second latches representing a single CAM memory cell;
third and fourth access transistors, each having a gate coupled to the word line to
which the first and second access transistors are coupled, the third and fourth access transistors
coupled between a data node of the second latch and a respective data line of the plurality; and
a second match circuit coupled to one of the complementary data nodes of the
second latch, the match circuit discharging the match line in response to a data value stored at the
data node to which the second match circuit is coupled and compare data present on the
respective data line mismatching.

15. The static CAM array of claim 14 wherein the first and second match
circuits comprise first and second switches, each switch having a control node and first and
second nodes, the first switch having its first node coupled to ground and its second node
coupled to the match line, and the second switch having its first node coupled to the first data
line, its second terminal coupled to the control terminal of the first switch, and its control node
coupled to the first data node.

16. The static CAM array of claim 14 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

17. The static CAM array of claim 12 wherein the latch comprises:

- a first switch having a first node coupled to a first of the complementary data nodes, a second node coupled to ground, and a control node coupled to the second data node;
- a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and
- first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

18. A content addressable memory (CAM) device, comprising:

- an address bus;
- a control bus;
- a data bus;
- an address decoder coupled to the address bus;
- a read/write circuit coupled to the data bus; and
- an array of CAM memory cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:
 - a plurality of word lines;
 - a plurality of data lines;
 - a latch having complementary data nodes capacitively coupled to ground;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit discharging a match line in response to a data value stored at the data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

19. The CAM device of claim 18 wherein the match circuit of the array of CAM memory cells comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

20. The CAM device of claim 18 wherein the latch of the array of CAM memory cells is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the

data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

21. The CAM device of claim 20 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node.

22. The CAM device of claim 20 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

23. The CAM device of claim 18 wherein the latch of the array of CAM memory cells comprises:

a first switch having a first node coupled to a first of the complementary data nodes, a second node coupled to ground, and a control node coupled to the second data node;

a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

24. A content addressable memory (CAM) device, comprising:
an address bus;

a control bus;
a data bus;
an address decoder coupled to the address bus;
a read/write circuit coupled to the data bus; and
an array of CAM memory cells coupled to the address decoder, control circuit, and read/write circuit, each CAM cell comprising:

a first bistable circuit coupled to a power supply and ground, the first bistable circuit having first and second data nodes;

a second bistable circuit coupled to the power supply and ground, the second bistable circuit having third and fourth data nodes;

first and second access transistors coupled to the first and second data nodes and first and second data lines, all respectively, for coupling the respective data node to the respective data line in response to activating a word line;

second and fourth access transistors coupled to the third and fourth data nodes and third and fourth data lines, all respectively, for coupling the respective data node to the respective data line in response to activating the word line;

first, second, third, and fourth capacitors, each capacitor having a first terminal coupled to a respective data node and having a second terminal coupled to ground; and

a match circuit having a first search node coupled to the first data line and a second search node coupled to the third data line, a first cell node coupled to the first data node and a second cell node coupled to the third data node, and a match node coupled to a match line, the match circuit changing the logic state of the match line in response to search data provided on the first data line and the first data node mismatch and search data provided on the third data line and the third data node mismatch.

25. The CAM device of claim 24 wherein the match circuit of the CAM cell comprises first, second, third, and fourth switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node

coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node, and the third switch having its first node coupled to ground and its second node coupled to the match line, and the fourth switch having its first node coupled to the third data line, its second terminal coupled to the control terminal of the third switch, and its control node coupled to the third data node.

26. The CAM device claim 24 wherein the match circuit off the CAM cell comprises first, second, third, and fourth switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor, and the third switch having its control terminal coupled to the third data node and its first node coupled to ground, the fourth switch having its control terminal coupled to the third data line, its first node coupled to the match line, and its second node coupled to the second node of the third transistor.

27. The CAM device of claim 24 wherein the first and second bistable circuits of the CAM cell comprise:

a first switch having a first node coupled to a true data node, a second node coupled to ground, and a control node coupled to a not data node;

a second switch having a first node coupled to the not data node, a second node coupled to ground, and a control node coupled to the true data node;

a first resistor having a first terminal coupled to the power supply and a second terminal coupled to the true data node; and

a second resistor having a first terminal coupled to the power supply and a second terminal coupled to the not data node.

28. The CAM device of claim 24 wherein the first and second data nodes of the CAM cell store complementary data, the first and second data lines are a pair of complementary data lines, the third and fourth data nodes store complementary data, and the third and fourth data lines are a pair of complementary data lines.

29. The CAM device of claim 24 wherein the search data and the data stored at the first data node are mismatching when the logic level of each are the same.

30. A computer system, comprising:
a data input device;
a data output device;
a processor coupled to the data input and output devices; and
a content addressable memory (CAM) device coupled to the processor, the CAM device comprising:

an address bus;
a control bus;
a data bus;
an address decoder coupled to the address bus;
a read/write circuit coupled to the data bus; and
an array of CAM memory cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;
a plurality of data lines;
a latch having complementary data nodes capacitively coupled to ground;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit discharging a match line in response to a data value stored at the data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

31. The computer system of claim 30 wherein the match circuit of the array of CAM memory cells comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

32. The computer system of claim 30 wherein the latch of the array of CAM memory cells is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

33. The computer system of claim 32 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node.

34. The computer system of claim 32 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

35. The computer system of claim 30 wherein the latch of the array of CAM memory cells comprises:

a first switch having a first node coupled to a first of the complementary data nodes, a second node coupled to ground, and a control node coupled to the second data node;

a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

36. A method for storing data in a content addressable memory, comprising:
charging a first node of a first capacitor;
activating a switch to couple a first node of a second capacitor to ground;
maintaining a charge at the first node of the first capacitor.

37. The method of claim 36 wherein maintaining a charge at the first node comprises providing charge to the first node of the first capacitor through a resistive current path.

38. The method of claim 36, further comprising coupling a resistive current path from a power supply to ground.

39. A method of storing data in a content addressable memory, comprising:
charging a first capacitor;
shunting a second capacitor; and
maintaining the charge on the first capacitor through a resistive current path.

40. The method of claim 39 wherein shunting the second capacitor comprises activating a switch to equalize the charge across the second capacitor.

41. A method for storing data in a content addressable memory, comprising:
charging a first capacitor;
setting a bistable circuit to a first state;
discharging a second capacitor in response to setting the bistable circuit; and
maintaining the charge on the first capacitor.

42. The method of claim 41 wherein maintaining the charge on the first capacitor comprises providing charge to the first capacitor through a resistive current path.